INTERNATIONAL TELECOMMUNICATION UNION

CCITT G.703

THE INTERNATIONAL
TELEGRAPH AND TELEPHONE
CONSULTATIVE COMMITTEE

GENERAL ASPECTS OF DIGITAL TRANSMISSION SYSTEMS

TERMINAL EQUIPMENTS

PHYSICAL/ELECTRICAL CHARACTERISTICS OF HIERARCHICAL DIGITAL INTERFACES

Recommendation G.703

Geneva, 1991

FOREWORD

The CCITT (the International Telegraph and Telephone Consultative Committee) is the permanent organ of the International Telecommunication Union (ITU). CCITT is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The Plenary Assembly of CCITT which meets every four years, establishes the topics for study and approves Recommendations prepared by its Study Groups. The approval of Recommendations by the members of CCITT between Plenary Assemblies is covered by the procedure laid down in CCITT Resolution No. 2 (Melbourne, 1988).

Recommendation G.703 was prepared by Study Group XVIII and was approved under the Resolution No. 2 procedure on the 5th of April 1991.

CCITT NOTES

1) In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication Administration and a recognized private operating agency.

2) A list of abbreviations used in this Recommendation can be found in Annex C.

Recommendation G.703

PHYSICAL/ELECTRICAL CHARACTERISTICS OF HIERARCHICAL DIGITAL INTERFACES

(Geneva, 1972; further amended)

The CCITT,

considering

that interface specifications are necessary to enable the interconnection of digital network components (digital sections, multiplex equipment, exchanges) to form an international digital link or connection;

that Recommendation G.702 defines the hierarchical levels;

that Recommendation G.704 deals with the functional characteristics of interfaces associated with network nodes;

that I.430-Series Recommendations deal with the layer 1 characteristics for ISDN user-network interfaces,

recommends

that physical and electrical characteristics of the interfaces at hierarchical bit rates be as described in this Recommendation.

Note 1 – The characteristics of interfaces at non-hierarchical bit rates, except $n \times 64$ kbit/s interfaces conveyed by 1544 kbit/s or 2048 kbit/s interfaces, are specified in the respective equipment Recommendations.

Note 2 – The jitter specifications contained in the following §§ 6, 7, 8 and 9 are intended to be imposed at international interconnection points.

Note 3 – The interfaces described in §§ 2 to 9 correspond to the ports T (output port) and T′ (input port) as recommended for interconnection in CCIR Recommendation AC/9 with reference to Report AH/9 of CCIR Study Group 9. (This Report defines the points T and T′.)

Note 4 – For signals with bit rates of $n \times 64$ kbit/s (n = 2 to 31) which are routed through multiplexing equipment specified for the 2048 kbit/s hierarchy, the interface shall have the same physical/electrical characteristics as those for the 2048 kbit/s interface specified in § 6. For signals with bit rates of $n \times 64$ kbit/s (n = 2 to 23) which are routed through multiplexing equipment specified for the 1544 kbit/s hierarchy, the interface shall have the same physical/electrical characteristics as those for the 1544 kbit/s interface specified in § 2.

1 Interface at 64 kbit/s

1.1 *Functional requirements*

1.1.1 The following basic requirements for the design of the interface are recommended:

1.1.2 In both directions of transmission, three signals can be carried across the interface:

- 64 kbit/s information signal,
- 64 kHz timing signal,
- 8 kHz timing signal.

Note 1 – The 64 kbit/s information signal and the 64 kHz timing signal are mandatory. However, although an 8 kHz timing must be generated by the controlling equipment (e.g. PCM multiplex or time slot access equipment), it should not be mandatory for the subordinate equipment on the other side of the interface to either utilize the 8 kHz timing signal from the controlling equipment or to supply an 8 kHz timing signal.

Note 2 – The detection of an upstream fault can be transmitted across the 64 kbit/s interface by transmitting an alarm indication signal (AIS) towards the subordinate equipment.

1.1.3 The interface should be bit sequence independent at 64 kbit/s.

Note 1 – An unrestricted 64 kbit/s signal can be transmitted across the interface. However, this does not imply that unrestricted 64 kbit/s paths are realizable on a global basis. This is because some Administrations presently have or are continuing to install extensive networks composed of digital line sections whose characteristics do not permit the transmission of long sequences of 0s. (Recommendation G.733 provides for PCM multiplexes with characteristics appropriate for such digital line sections.) Specifically for octet timed sources, in 1544 kbit/s digital networks it is required that at least one binary 1 should be contained in any octet of a 64 kbit/s digital signal. For a bit stream which is not octet timed no more than 7 consecutive 0s should appear in the 64 kbit/s signal.

Note 2 – Although the interface is bit sequence independent, the use of the AIS (all 1s bit pattern) may result in some minor restrictions for the 64 kbit/s source. For example, an all 1s alignment signal could result in problems.

1.1.4 *Three types of envisaged interfaces*

1.1.4.1 *Codirectional interface*

The term codirectional is used to describe an interface across which the information and its associated timing signal are transmitted in the same direction (see Figure 1/G.703).

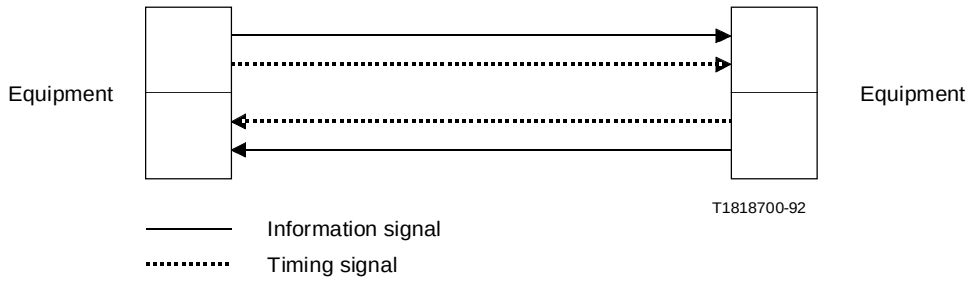


FIGURE 1/G.703
Codirectional interface

1.1.4.2 *Centralized clock interface*

The term centralized clock is used to describe an interface wherein for both directions of transmission of the information signal, the associated timing signals are supplied from a centralized clock, which may be derived for example from certain incoming line signals (see Figure 2/G.703).

Note – The codirectional interface or centralized clock interface should be used for synchronized networks and for plesiochronous networks having clocks of the stability required (see Recommendation G.811) to ensure an adequate interval between the occurrence of slips.

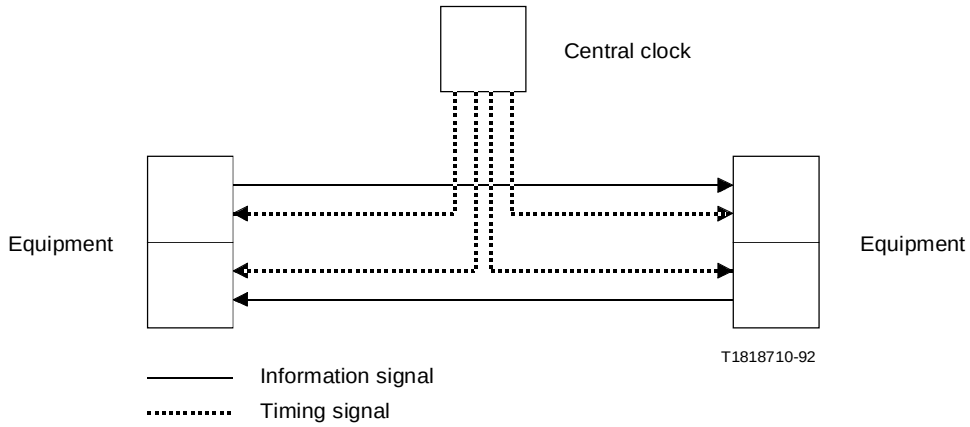


FIGURE 2/G.703

Centralized clock interface

1.1.4.3 *Contradirectional interface*

The term contradirectional is used to describe an interface across which the timing signals associated with both directions of transmission are directed towards the subordinate equipment (see Figure 3/G.703).

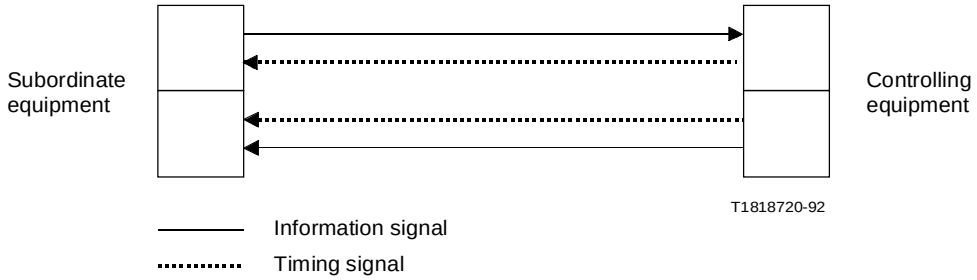


FIGURE 3/G.703

Contradirectional interface

1.2 *Electrical characteristics*

1.2.1 *Electrical characteristics of 64 kbit/s codirectional interface*

1.2.1.1 *General*

1.2.1.1.1 Nominal bit rate: 64 kbit/s.

1.2.1.1.2 Maximum tolerance of signals to be transmitted through the interface: ± 100 ppm.

1.2.1.1.3 64 Hz and 8 kHz timing signal to be transmitted in a codirectional way with the information signal.

1.2.1.1.4 One balanced pair for each direction of transmission; the use of transformers is recommended.

1.2.1.1.5 *Code conversion rules*

Step 1 – A 64 kbit/s bit period is divided into four unit intervals.

Step 2 – A binary one is coded as a block of the following four bits:

1 1 0 0

Step 3 – A binary zero is coded as a block of the following four bits:

1 0 1 0

Step 4 – The binary signal is converted into a three-level signal by alternating the polarity of consecutive blocks.

Step 5 – The alternation in polarity of the blocks is violated every 8th block. The violation block marks the last bit in an octet.

These conversion rules are illustrated in Figure 4/G.703.

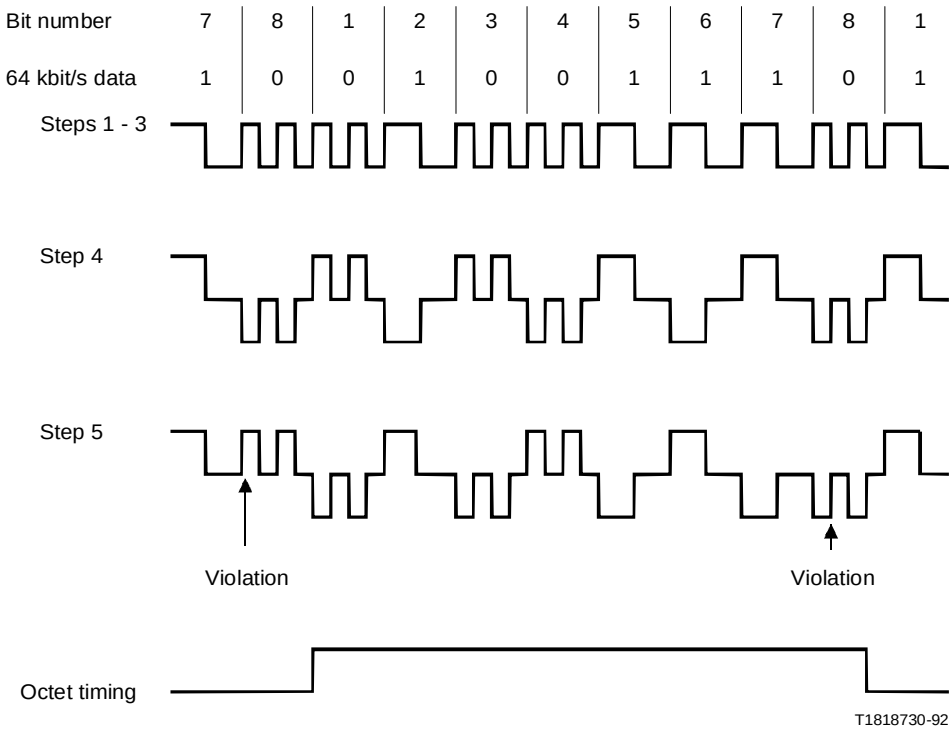


FIGURE 4/G.703

Illustration of the conversion rules

1.2.1.1.6 *Overvoltage protection requirement*

See Annex B.

1.2.1.2 *Specifications at the output ports*

See Table 1/G.703.

1.2.1.3 *Specifications at the input ports*

The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of these pairs at a frequency of 128 kHz should be in the range 0 to 3 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

The return loss at the input ports should have the following minimum values:

Frequency range (kHz)	Return loss (dB)
4 to 13	12
13 to 256	18
256 to 384	14

To provide nominal immunity against interference, input ports are required to meet the following requirements:

A nominal aggregate signal, encoded as a 64 kbit/s codirectional signal and having a pulse shape as defined in the pulse mask, shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 120 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with Recommendation O.152 ($2^{11} - 1$ bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

Note – If the symmetrical pair is screened, the screen shall be connected to the earth at the output port, and provision shall be made for connecting the screen of the symmetrical pair to earth, if required, at the input port.

1.2.2 *Electrical characteristics of the 64 kbit/s centralized clock interface*

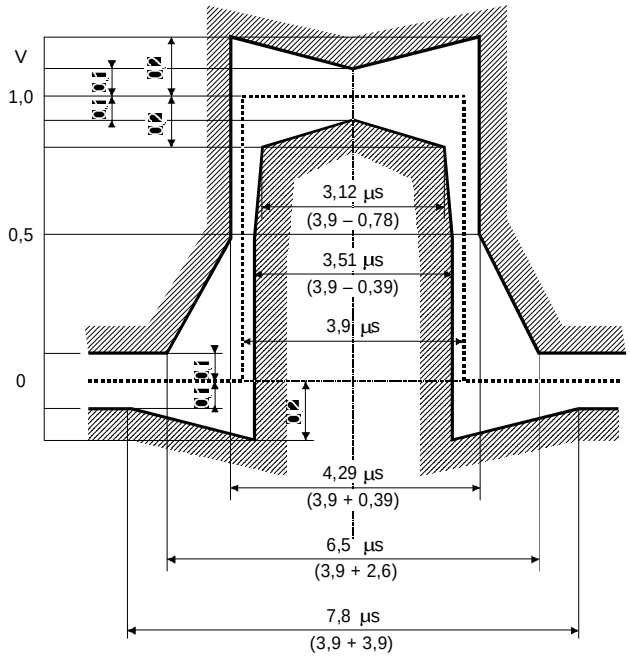
1.2.2.1 *General*

1.2.2.1.1 Nominal bit rate: 64 kbit/s. The tolerance is determined by the network clock stability (see Recommendation G.811).

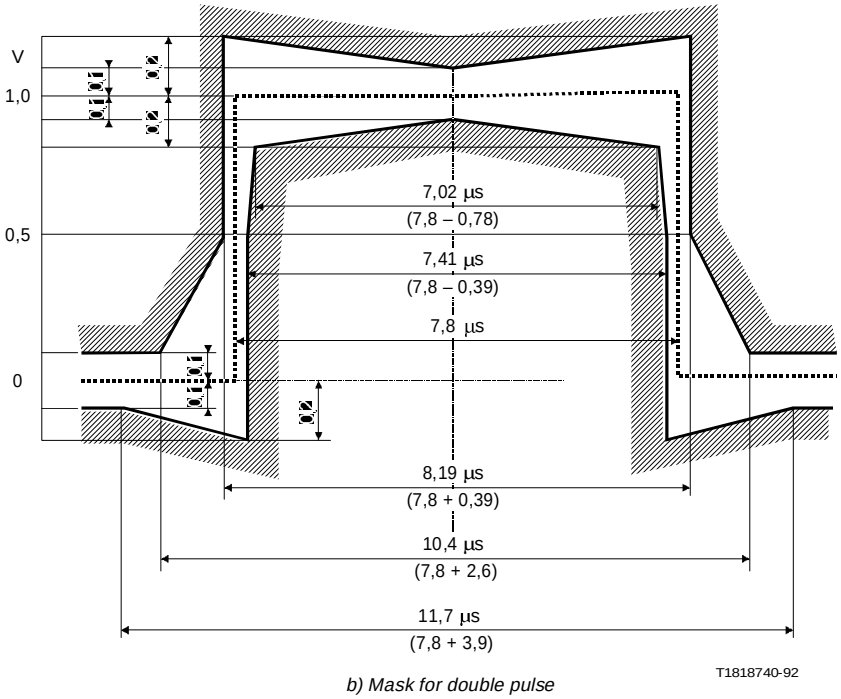
1.2.2.1.2 For each direction of transmission there should be one symmetrical pair carrying the data signal. In addition, there should be symmetrical pairs carrying the composite timing signal (64 kHz and 8 kHz) from the central clock source to the office terminal equipment. The use of transformers is recommended.

1.2.2.1.3 *Overvoltage protection requirement*

See Annex B.



a) Mask for single pulse



b) Mask for double pulse

Note – The limits apply to pulses of either polarity.

FIGURE 5/G.703

Pulse masks of the 64 kbit/s codirectional interface

TABLE 1/G.703

Symbol rate	256 kbauds
Pulse shape (nominally rectangular)	All pulses of a valid signal must conform to the masks in Figure 5/G.703, irrespective of the polarity
Pair for each direction	One symmetric pair
Test load impedance	120 ohms resistive
Nominal peak voltage of a “mark” (pulse)	1.0 V
Peak voltage of a “space” (no pulse)	0V ± 0.10 V
Nominal pulse width	3.9 μs
Ratio of the amplitudes of positive and negative pulses at the centre of the pulses interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Maximum peak-to-peak jitter at the output port (Note)	Refer to § 2 of Recommendation G.823

Note – For the time being these values are valid only for equipments of the 2 Mbit/s hierarchy.

1.2.2.1.4 *Code conversion rules*

The data signals are coded in AMI code with a 100% duty ratio. The composite timing signals convey the 64 kHz bit-timing information using AMI code with a 50% to 70% duty ratio and the 8 kHz octet-phase information by introducing violations of the code rule. The structure of the signals and their nominal phase relationships are shown in Figure 6/G.703.

The data stream at the output ports should be timed by the leading edge of the timing pulse and the detection instant at the input ports should be timed by the trailing edge of each timing pulse.

1.2.2.2 *Characteristics at the output ports*

See Table 2/G.703.

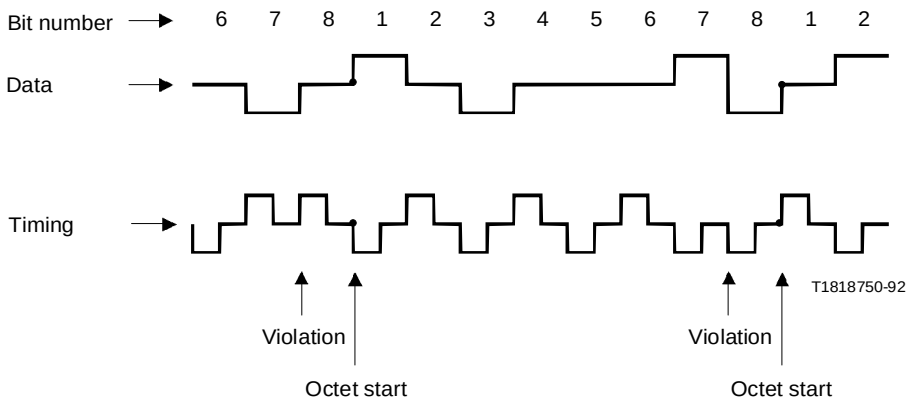


FIGURE 6/G.703

Signal structures of the 64-kbit/s central clock interface at office terminal output ports

TABLE 2/G.703

Parameters	Data	Timing
Pulse shape	Nominally Rectangular, with rise and fall times less than 1 µsec	Nominally Rectangular, with rise and fall times less than 1 µsec
Nominal test load impedance	110 ohms resistive	110 ohms resistive
Peak voltage of a “mark” (pulse) (Note 1)	a) 1.0 ± 0.1 V b) 3.4 ± 0.5 V	a) 1.0 ± 0.1 V b) 3.0 ± 0.5 V
Peak value of a “space” (no pulse) (Note 1)	a) 0 ± 0.1 V b) 0 ± 0.5 V	a) 0 ± 0.1 V b) 0 ± 0.5 V
Nominal pulse width (Note 1)	a) 15.6 µs b) 15.6 µs	a) 7.8 µs b) 9.8 to 10.9 µs
Maximum peak-to-peak jitter at the output port (Note 2)	Refer to § 2 of Recommendation G.823	

Note 1 – The choice between the set of parameters a) and b) allows for different office noise environments and different maximum cable lengths between the three involved office equipments.

Note 2 – For the time being these values are valid only for equipments of the 2 Mbit/s hierarchy.

1.2.2.3 *Characteristics at the input ports*

The digital signals presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pairs. The varying parameters in Table 2/G.703 will allow typical maximum interconnecting distances of 350 to 450 m.

1.2.2.4 *Cable characteristics*

The transmission characteristics of the cable to be used are subject to further study.

1.2.3 *Electrical characteristics of 64 kbit/s contradirectional interface*

1.2.3.1 *General*

1.2.3.1.1 Bit rate: 64 kbit/s.

1.2.3.1.2 Maximum tolerance for signals to be transmitted through the interface: ± 100 ppm.

1.2.3.1.3 For each direction of transmission there should be two symmetrical pairs of wires, one pair carrying the data signal and the other carrying a composite timing signal (64 kHz and 8 kHz). The use of transformers is recommended.

Note – If there is a national requirement to provide a separate alarm signal across the interface, this can be done by cutting the 8 kHz timing signal for the transmission direction concerned, i.e., by inhibiting the code violations introduced in the corresponding composite timing signal (see below).

1.2.3.1.4 *Code conversion rules*

The data signals are coded in AMI code with a 100% duty ratio. The composite timing signals convey the 64 kHz bit-timing information using AMI code with a 50% duty ratio and the 8 kHz octet-phase information by introducing violations of the code rule. The structures of the signals and their phase relationships at data output ports are shown in Figure 7/G.703.

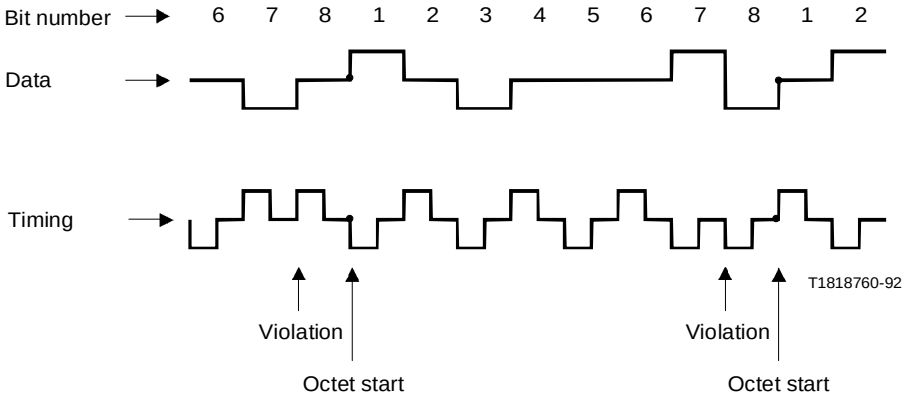


FIGURE 7/G.703

Signal structures of the 64-kbit/s contradirectional interface at data output ports

The data pulses received from the service (e.g. data or signalling) side of the interface will be somewhat delayed in relation to the corresponding timing pulses. The detection instant for a received data pulse on the line side (e.g. PCM) of the interface should therefore be at the leading edge of the next timing pulse.

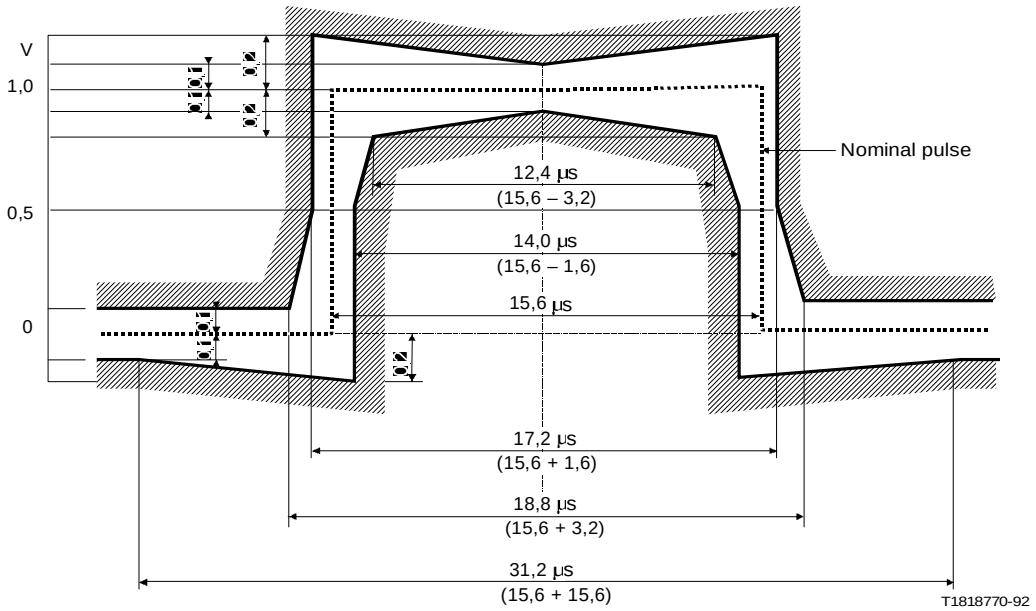
1.2.3.1.5 *Specifications at the output ports*

See Table 3/G.703.

TABLE 3/G.703

Parameters	Data	Timing
Pulse shape (nominally rectangular)	All pulses of a valid signal must conform to the mask in Figure 8/G.703 irrespective of the polarity	All pulses of a valid signal must conform to the mask in Figure 9/G.703, irrespective of the polarity
Pairs in each direction of transmission	One symmetric pair	One symmetric pair
Test load impedance	120 ohms resistive	120 ohms resistive
Nominal peak voltage of a “mark” (pulse)	1.0 V	1.0 V
Peak voltage of a “space” (no pulse)	0 V ± 0.1 V	0 V ± 0.1 V
Nominal pulse width	15.6 µs	7.8 µs
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	0.95 to 1.05
Maximum peak-to-peak jitter at the output port (Note)	Refer to § 2 of Recommendation G.823	

Note – For the time being these values are valid only for equipments of the 2 Mbit/s.



Note 1 – When one pulse is immediately followed by another pulse of the opposite polarity, the time limits at the zero-crossing between the pulses should be ± 0.8 µs.

Note 2 – The time instants at which a transition from one state to another in the data signal may occur are determined by the timing signal. On the service (e.g. data or signalling) side of the interface it is essential that these transitions are not initiated in advance of the timing instants given by the received timing signal.

FIGURE 8/G.703

Mask of the data pulse of the 64-kbit/s contradirectional interface

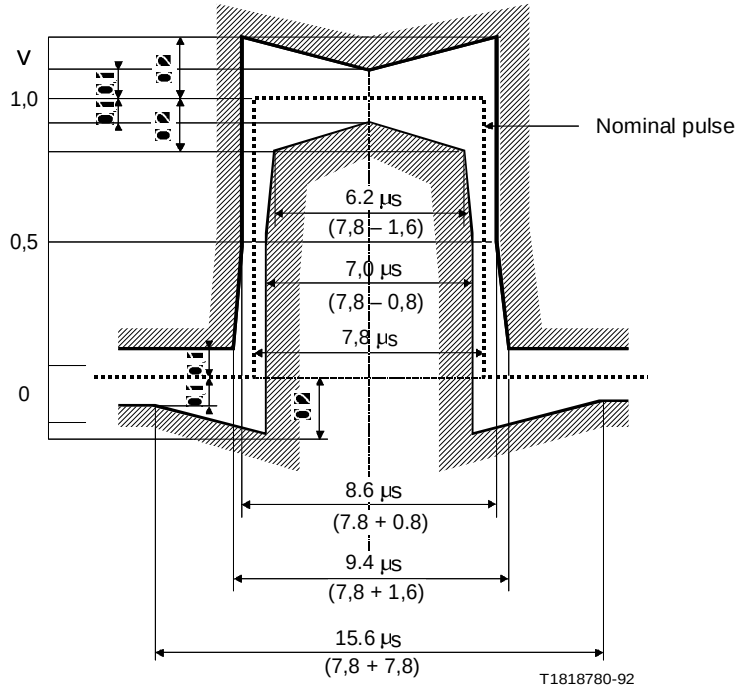


FIGURE 9/G.703

Mask of the timing pulse of the 64-kbit/s contradirectional interface

1.2.3.1.6 *Specifications at the input ports*

The digital signals presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of these pairs at a frequency of 32 kHz should be in the range 0 to 3 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

The return loss at the input ports should have the following minimum values:

Frequency range (kHz)		Return loss (dB)
Data signal	Composite timing signal	
1.6 to 3.2 3.2 to 64 64 to 96	3.2 to 6.4 6.4 to 128 128 to 192	12 18 14

To provide nominal immunity against interference, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded as a 64 kbit/s contra-directional signal and having a pulse shape as defined in the pulse mask, shall have added to it an intefering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 120 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with Recommendation O.152 (2^{11} – 1 bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

Note 1 – The return loss specification for both the data signal and the composite timing signal input ports.

Note 2 – If the symmetrical pairs are screened, the screens shall be connected to the earth at the output port, and provision shall be made for connecting the screens of the symmetrical pairs to earth, if required, at the input port.

1.2.3.1.7 *Overvoltage protection requirement*

See Annex B.

2 Interface at 1544 kbit/s

2.1 Interconnection of 1544 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

2.2 The signal shall have a bit rate of 1544 kbit/s ± 50 parts per million (ppm).

2.3 One symmetrical pair shall be used for each direction of transmission.

2.4 Test load impedance shall be 100 ohms, resistive.

2.5 An AMI (bipolar) code or B8ZS code shall be used. Connecting line systems require suitable signal content to guarantee adequate timing information. This can be accomplished either by use of B8ZS code, scrambling or by permitting not more than 15 spaces between successive marks and having an average mark density of at least 1 in 8.

2.6 The shape for an isolated pulse measured at the distribution frame shall fall within the mask in Figure 10/G.703 and meet the other requirements of Table 4/G.703. For pulse shapes within the mask, the peak undershoot should not exceed 40% of the peak pulse (mark).

2.7 The voltage within a time slot containing a zero (space) shall be no greater than either the value produced in that time slot by other pulses (marks) within the mask of Figure 10/G.703 or ± 0.1 of the peak pulse (mark) amplitude, whichever is greater in magnitude.

3 Interface at 6312 kbit/s

3.1 Interconnection of 6312 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

3.2 The signal shall have a bit rate of 6312 kbit/s ± 30 ppm.

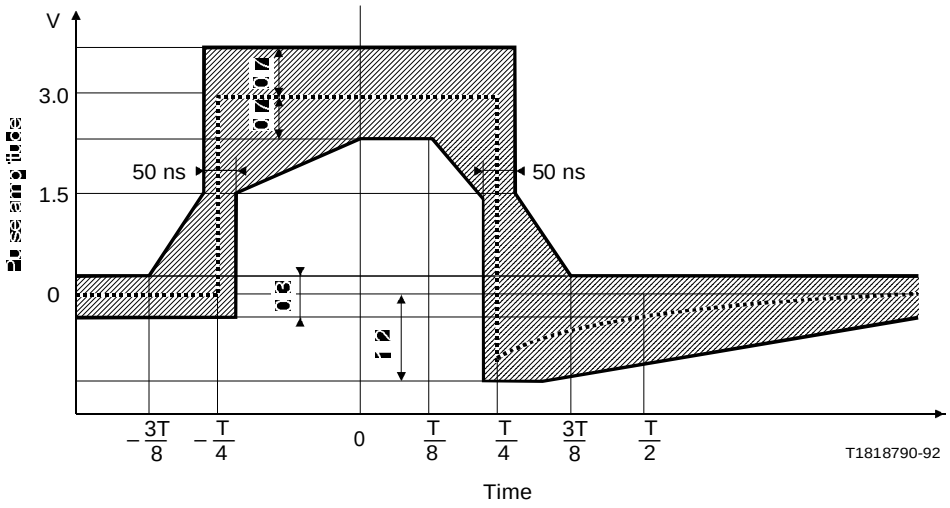
3.3 One symmetrical pair of characteristic impedance of 110 ohms, or one coaxial pair of characteristic impedance of 75 ohms shall be used for each direction of transmission.

3.4 Test load impedance shall be 110 ohms resistive or 75 ohms resistive as appropriate.

3.5 A pseudo-ternary code shall be used as indicated in Table 5/G.703.

3.6 The shape for an isolated pulse measured at the distribution frame shall fall within the mask either of Figure 11/G.703 or of Figure 12/G.703 and meet the other requirements of Table 5/G.703.

3.7 The voltage within a time slot containing a zero (space) shall be no greater than either the value produced in that time slot by other pulses (marks) within the mask of Figure 11/G.703, or ± 0.1 of the peak pulse (mark) amplitude, whichever is greater in magnitude.



T Time-slot width

FIGURE 10/G.703

Pulse mask for interface at 1544 kbit/s

TABLE 4/G.703

Digital interface at 1544 kbits a)

Location		Digital distribution frame
Bit rate		1544 kbit/s
Pair(s) in each direction of transmission		One symmetric pair
Code		AMI b) or B8ZS c)
Test load impedance		100 ohms resistive
Nominal pulse shape		Rectangular
Signal level d)	Power at 772 kHz	+ 12 dBm to + 19 dBm
	Power to 1544 kHz	At least 25 dB below the power at 772 kHz

a) The pulse mask for 1st order digital interface is shown in Figure 10/G.703

b) See § 2.5 in the text.

c) See Annex A.

d) The signal level is the power level measured in a 3 kHz bandwidth at the point where the signal arrives at the distribution frame for an all 1s pattern transmitted.

TABLE 5/G.703

Digital interface at 6312 kbit/s a)

Location	Digital distribution frame	
Bit rate	6312 kbit/s	
Pair(s) in each direction of transmission	One symmetric pair	One coaxial pair
Code	B6ZS b)	B8ZS b)
Test load impedance	110 ohms resistive	75 ohms resistive
Nominal pulse shape a)	Rectangular, shaped by cable loss (see Figure 11/G.703)	Rectangular (see Figure 12/G.703)
Signal level	For an all 1 s pattern transmitted, the power measured in a 3-kHz bandwidth should be as follows:	
	3156 kHz: 0.2 to 7.3 dBm 6312 kHz: –20 dBm or less	3156 kHz: 6.2 to 13.3 dBm 6312 kHz: –14 dBm or less

a) The pulse mask for 2nd order digital interface is shown in Figures 1/G.703 and 12/G.703·

b) See Annex A.

4 Interface at 32 064 kbit/s

4.1 Interconnection of 32 064 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

4.2 The signal shall have a bit rate of 32 064 kbit/s ± 10 ppm.

4.3 One coaxial pair shall be used for each direction of transmission.

4.4 The test load impedance shall be 75 ohms ± 5 per cent resistive and the test method shall be direct.

	T	Value of curve
Lower curve	$T \leq -0.41$ $-0.41 \leq T \leq 0.24$ $0.24 \leq T$	0 $0.5 \left[1 + \sin \frac{\pi}{2}\left(1 + \frac{T}{0.205}\right)\right]$ $0.331\, e^{-1.9\,(T - 0.3)}$
Upper curve	$T \leq -0.72$ $-0.72 \leq T \leq 0.2$ $0.2 \leq T$	0 $0.5 \left[1 + \sin \frac{\pi}{2}\left(1 + \frac{T}{0.36}\right)\right]$ $0.1 + 0.72\, e^{-2.13\,(T - 0.2)}$

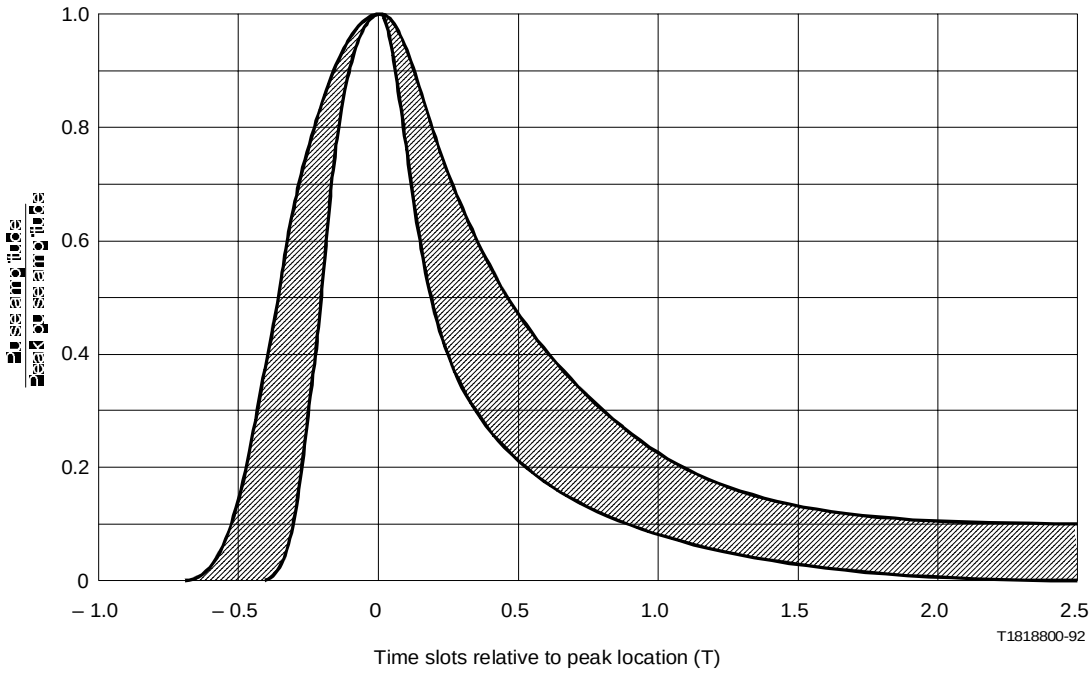


FIGURE 11/G.703

Pulse mask for the symmetric pair interface at 6312 kbit/s

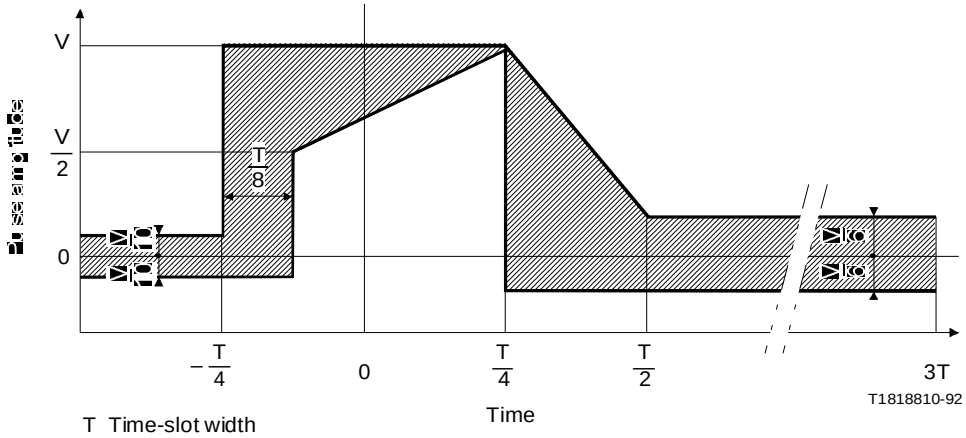


FIGURE 12/G.703

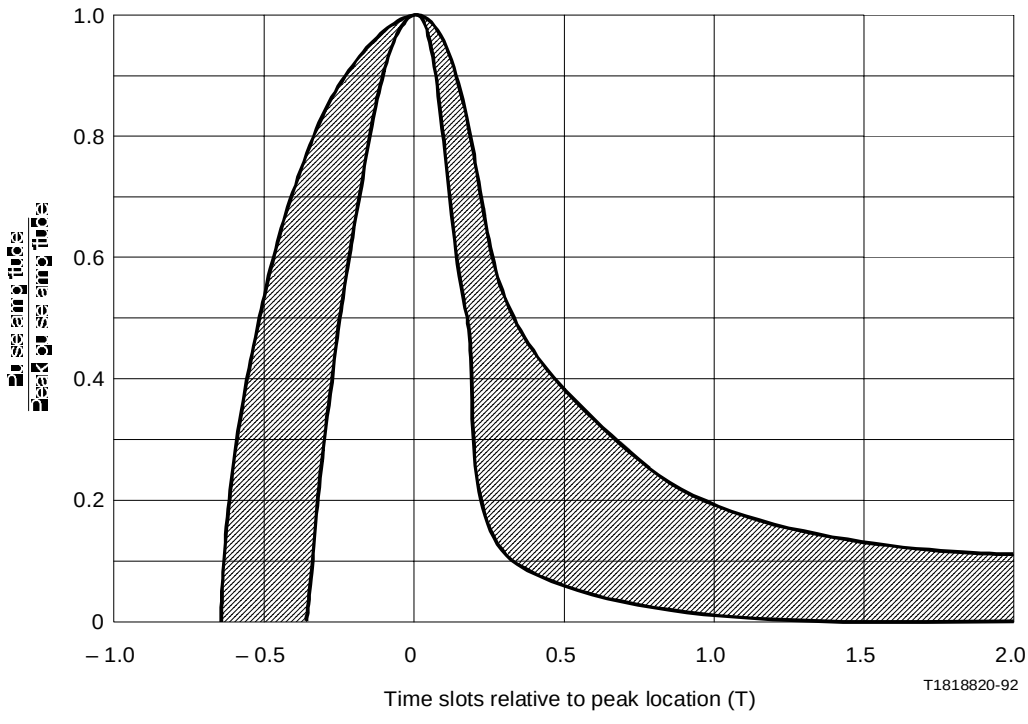
Pulse mask for the coaxial pair interface at 6312 kbit/s

4.5 A scrambled AMI code shall be used.

4.6 The shape for an isolated pulse measured at the point where the signal arrives at the distribution frame shall fall within the mask in the Figure 13/G.703.

4.7 The voltage within a time slot containing a zero (space) shall be no greater than either the value produced in that time slot by other pulses (marks) within the mask of Figure 13/G.703 or ± 0.1 of the peak pulse (mark) amplitude, whichever is greater in magnitude.

	T	Value of curve
Lower curve	$-0.36 \leq T < -0.30$	$5.76\ T + 2.07$
	$-0.30 \leq T < 0$	$0.5 \left[1 + \sin \frac{\pi}{2}\left(1 + \frac{T}{0.25}\right)\right]$
	$0 \leq T < 0.22$	$0.5 \left[1 + \sin \frac{\pi}{2}\left(1 + \frac{T}{0.16}\right)\right]$
	$0.22 \leq T$	$0.11\ e^{-3.42\ (T - 0.3)}$
Upper curve	$-0.65 \leq T < 0$	$1.05 \left[1 - e^{-4.6\ (T + 0.65)}\right]$
	$0 \leq T < 0.25$	$0.5 \left[1 + \sin \frac{\pi}{2}\left(1 + \frac{T}{0.28}\right)\right]$
	$0.25 \leq T$	$0.11 + 0.407\ e^{-2.1\ (T - 0.29)}$



FIGUR E 13/G.703

Pulse mask for the coaxial pair interface at 32 064 kbit/s

4.8 For an all 1s pattern transmitted, the power measured in a 3 kHz bandwidth at the point where the signal arrives at the distribution frame shall be as follows:

16 032 kHz: +5 dBm to +12 dBm

32 064 kHz: at least 20 dB below the power at 16 032 kHz.

4.9 The connectors and coaxial cable pairs in the distribution frame shall be 75 ohms ± 5 per cent.

5 Interface at 44 736 kbit/s

5.1 Interconnection of 44 736 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

5.2 The signal shall have a bit rate of 44 736 kbit/s ± 20 ppm.

The signal shall have a frame structure consistent with Recommendation G.752. Specifically, it shall contain the frame alignment bits F_0, F_{11}, F_{12} and the multi-frame alignment bits M_1 to M_7, as defined in Table 2/G.752.

5.3 One coaxial pair shall be used for each direction of transmission.

5.4 Test load impedance shall be 75 ohms ± 5 per cent resistive, and the test method shall be direct.

5.5 The B3ZS code shall be used. This code is defined in Annex A.

5.6 The transmitted pulses have a nominal 50% duty cycle.

The shape for an isolated pulse measured at the point where the signal arrives at the distribution frame shall fall within the mask in Figure 14/G.703.

5.7 The voltage within a time slot containing a zero (space) shall be no greater than either the value produced in that time slot by other pulses (marks) within the mask of Figure 14/G.703, or ± 0.05 of the peak pulse (mark) amplitude, whichever is greater in magnitude.

5.8 For an all 1s pattern transmitted, the power measured in a 3 kHz bandwidth at the point where the signal arrives at the distribution frame shall be as follows:

22 368 kHz: –1.8 to +5.7 dBm

44 736 kHz: at least 20 dB below the power at 22 368 kHz.

5.9 The digital distribution frame for 44 736 kbit/s signals shall have the characteristics specified in §§ 5.9.1 and 5.9.2 below.

5.9.1 The loss between the points where the signal arrives and leaves at the distribution frame shall be as follows:

0.60 ± 0.55 dB at 22 368 kHz

(comprised of any combination of flat and shaped losses).

5.9.2 The connectors and coaxial pair cables in the distribution frame shall be 75 ohms ± 5 per cent.

6 Interface at 2048 kbit/s

6.1 *General characteristics*

Bit rate: 2048 kbit/s ± 50 ppm

Code: High density bipoler of order 3 (HDB3) (a description of this code can be found in Annex A).

Overvoltage protection requirement: see Annex B.

6.2 *Specifications at the output ports*

See Table 6/G.703.

6.3 *Specifications at the input ports*

6.3.1 The digital signal presented at the input port shall be as defined above but modified by the characteristic of the interconnecting pair. The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 1024 kHz shall be in the range 0 to 6 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

6.3.2 For the jitter to be tolerated at the input port, refer to § 3 of Recommendation G.823.

	T	Value of curve
Lower curve	$T \leq -0.36$	0
	$-0.36 \leq T \leq 0.28$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right]$
	$0.28 \leq T$	$0.11\, e^{-3.42\,(T - 0.3)}$
Upper curve	$T \leq -0.65$	0
	$-0.65 \leq T \leq 0$	$1.05\left[1 - e^{-4.6(T + 0.65)}\right]$
	$0 \leq T \leq 0.36$	$0.5\left[1 + \sin\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right]$
	$0.36 \leq T$	$0.05 + 0.407\, e^{-1.84\,(T - 0.36)}$

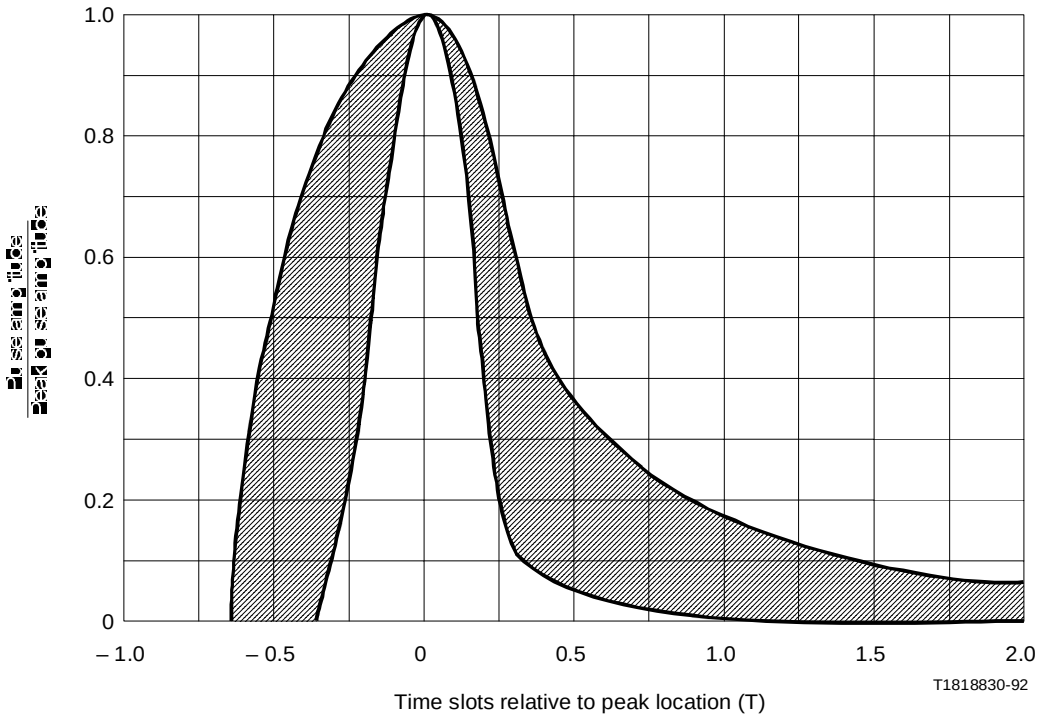


FIGURE 14/G.703

Pulse mask for the coaxial pair interface at 44 736 kbit/s

TABLE 6/G.703

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Figure 15/G.703) irrespective of the sign. The value V corresponds to the nominal peak value.	
Pair(s) in each direction	One coaxial pair (see § 6.4)	One symmetrical pair (see § 6.4)
Test load impedance	75 ohms resistive	120 ohms resistive
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	
Maximum peak-to-peak jitter at an output port	Refer to § 2 of Recommendation G.823	

6.3.3 The return loss at the input port should have the following provisional minimum values:

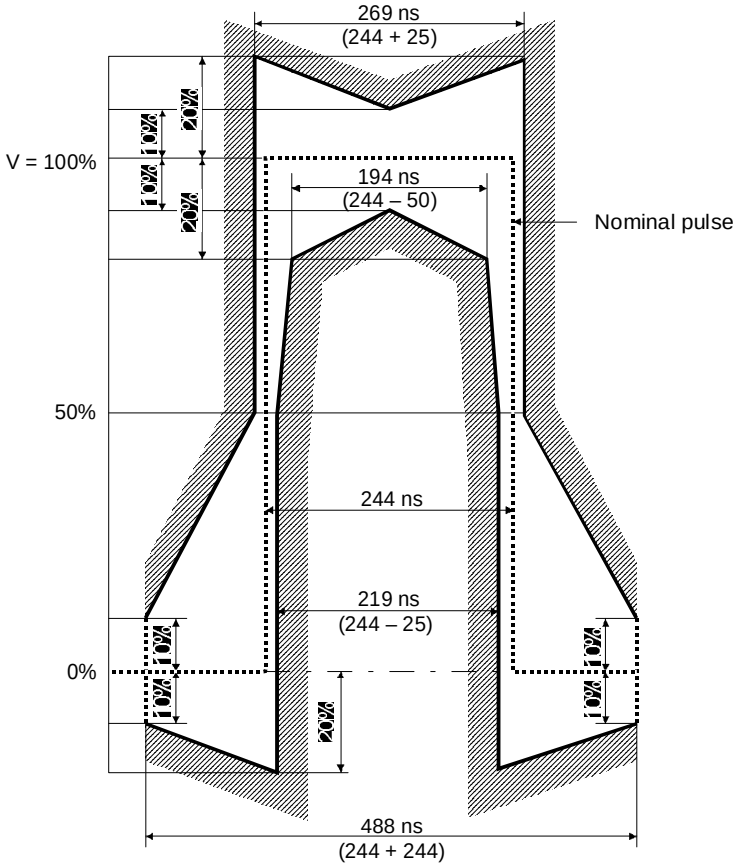
Frequency range (kHz)	Return loss (dB)
51 to 102 102 to 2048 2048 to 3072	12 18 14

6.3.4 To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask, shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms (in the case of coaxial-pair interface) or 120 ohms (in

the case of symmetrical-pair interface), to give a signal-to-interference ratio of 18 dB. The binary content of the interfering signal should comply with Recommendation O.151 (2^{15} – 1 bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

Note – A receiver implementation providing an adaptive rather than a fixed threshold is considered to be more robust against reflections and should therefore be preferred.



Note – V corresponds to the nominal peak value.

FIGURE 15/G.703

Mask of the pulse at the 2048 kbit/s interface

6.4 *Earthing of outer conductor or screen*

The outer conductor of the coaxial pair or the screen of the symmetrical pair shall be connected to the earth at the output port and provision shall be made for connecting the outer conductor of the coaxial pair or the screen of the symmetrical pair to earth if required, at the input port.

7 Interface at 8448 kbit/s

7.1 *General characteristics*

Bit rate: 8448 kbit/s ± 30 ppm

Code: HDB3 (a description of this code can be found in Annex A).

Overvoltage protection requirement: see Annex B.

7.2 *Specification at the output ports*

See Table 7/G.703.

TABLE 7/G.703

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (Figure 16/G.703) irrespective of the sign
Pair(s) in each direction	One coaxial pair (see § 7.4)
Test load impedance	75 ohms resistive
Nominal peak voltage of a mark (pulse)	2.37 V
Peak voltage of a space (no pulse)	0 V ± 0.237 V
Nominal pulse width	59 ns
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05
Ratio of widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Maximum peak-to-peak jitter at an output port	Refer to § 2 of Recommendation G.823

7.3 *Specifications at the input ports*

7.3.1 The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 4224 kHz shall be in the range 0 to 6 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

7.3.2 For the jitter to be tolerated at the input port, refer to § 3 of Recommendation G.823.

7.3.3 The return loss at the input port should have the following provisional minimum values:

Frequency range (kHz)	Return loss (dB)
211 to 422	12
422 to 8 448	18
8 448 to 12 672	14

7.3.4 To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with Recommendation O.151 (2^{15} – 1 bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

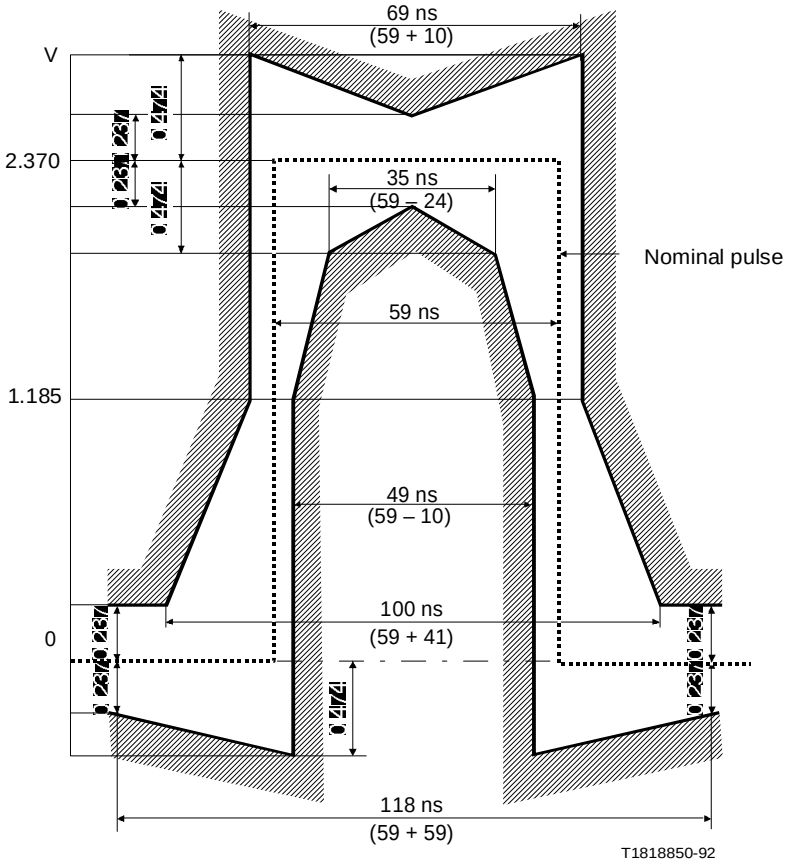


FIGURE 16/G.703

Pulse mask at the 8448-kbit/s interface

7.4 *Earthing of outer conductor or screen*

The outer conductor of the coaxial pair shall be connected to the earth at the output port, and provision shall be made for connecting this conductor to earth, if required, at the input port.

8 Interface at 34 368 kbit/s

8.1 *General characteristics*

Bit rate: 34 368 kbit/s ± 20 ppm

Code: HDB3 (a description of this code can be found in Annex A).

Overvoltage protection requirement: see Annex B.

8.2 *Specification at the output ports*

See Table 8/G.703.

8.3 *Specifications at the input ports*

8.3.1 The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pair. The attenuation of this cable shall be assumed to follow approximately a $\sqrt{f}$ law and the loss at a frequency of 17 184 kHz shall be in the range 0 to 12 dB.

8.3.2 For the jitter to be tolerated at the input port, refer to § 3 of Recommendation G.823.

8.3.3 The return loss at the input port should have the following provisional minimum values:

Frequency range (kHz)	Return loss (dB)
860 to 1 720	12
1 720 to 34 368	18
34 368 to 51 550	14

8.3.4 To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with Recommendation O.151 ($2^{23} - 1$ bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

8.4 *Earthing of outer conductor or screen*

The outer conductor of the coaxial pair shall be connected to the earth at the output port, and provision shall be made for connecting this conductor to earth, if required, at the input port.

TABLE 8/G.703

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Figure 17/G.703), irrespective of the sign
Pair(s) in each direction	One coaxial pair (see § 8.4)
Test load impedance	75 ohms resistive
Nominal peak voltage of a mark (pulse)	1.0 V
Peak voltage of a space (no pulse)	0 V ± 0.1 V
Nominal pulse width	14.55 ns
Ratio of the amplitudes of positive and negative pulses at the center of a pulse interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Maximum peak-to-peak jitter at an output port	Refer to § 2 of Recommendation G.823

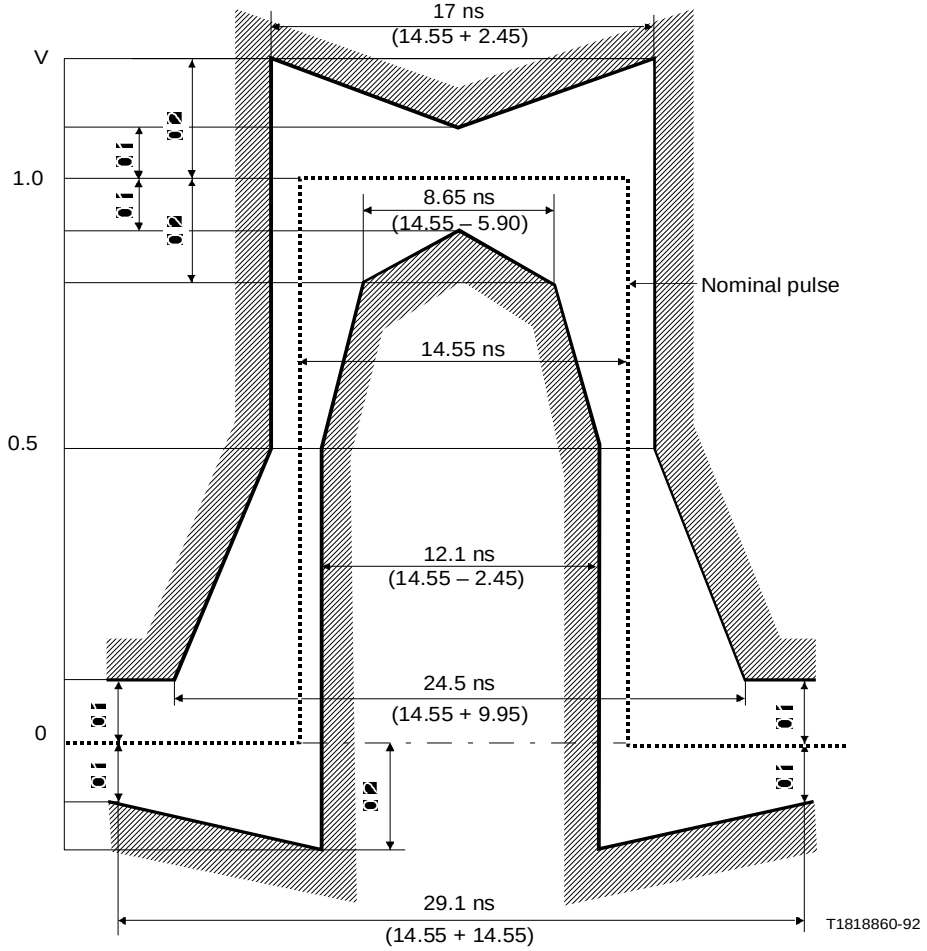


FIGURE 17/G.703

Pulse mask at the 34 368-kbit/s interface

9 Interface at 139 264 kbit/s

9.1 *General characteristics*

Bit rate: 139 264 kbit/s ± 15 ppm

Code: coded mark inversion (CMI)

Overvoltage protection requirement: see Annex B.

CMI is a 2-level non-return-to-zero code in which binary 0 is coded so that both amplitude levels, A_1 and A_2, are attained consecutively, each for half a unit time interval (T/2).

Binary 1 is coded by either of the amplitude levels A_1 or A_2, for one full unit time interval (T), in such a way that the level alternates for successive binary 1s.

An example is given in Figure 18/G.703.

Note 1 – For binary 0, there is always a positive transition at the midpoint of the binary unit time interval.

Note 2 – For binary 1,

a) there is a positive transition at the start of the binary unit time interval if in the preceeding time interval the level was A_1;

b) there is a negative transition at the start of the binary unit time interval if the last binary 1 was encoded by level A_2.

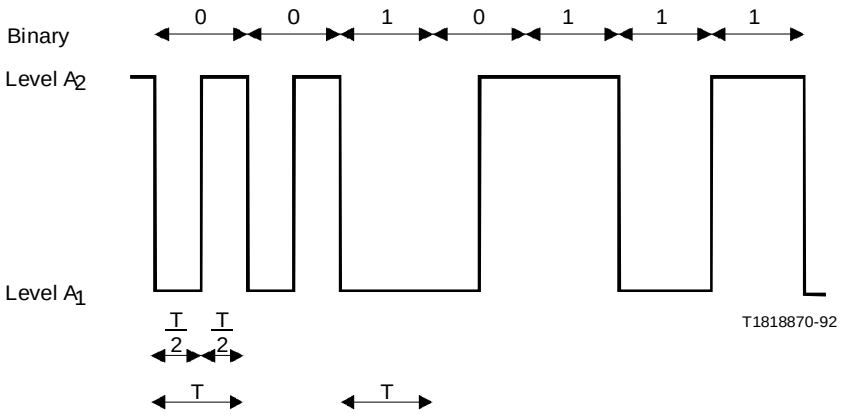


FIGURE 18/G.703

Example of CMI coded binary signal

9.2 *Specifications at the output ports*

The specifications at the output ports are given in Table 9/G.703 and Figures 19/G.703 and 20/G.703.

Note – A method based on the measurement of the levels of the fundamental frequency component, the second (and possibly the third) harmonic of a signal corresponding to binary all 0s and binary all 1s, is considered to be a perfectly adequate method of checking that the requirements of Table 9/G.703 have been met. The relevant values of the harmonic components are under study.

TABLE 9/G.703

Pulse shape	Nominally rectangular and conforming to the masks shown in Figures 19/G.703 and 20/G.703
Pair(s) in each direction	One coaxial pair
Test load impedance	75 ohms resistive
Peak-to-peak voltage	1 ± 0.1 V
Rise time between 10% and 90% amplitudes of the measured steady state amplitude	≤ 2 ns
Transition timing tolerance (referred to the mean value of the 50% amplitude points of negative transitions)	Negative transitions:: ± 0.1 ns Positive transitions at unit interval boundaries: ± 0.5 ns Positive transitions at mid-interval: ± 0.35 ns
Return loss	≥ 15 dB over frequency range 7 MHz to 210 MHz
Maximum peak-to-peak jitter at an output port	Refer to § 2 of Recommendation G.823

9.3 *Specifications at the input ports*

The digital signal presented at the input port should conform to Table 9/G.703 and Figures 19/G.703 and 20/G.703 modified by the characteristics of the interconnecting coaxial pair.

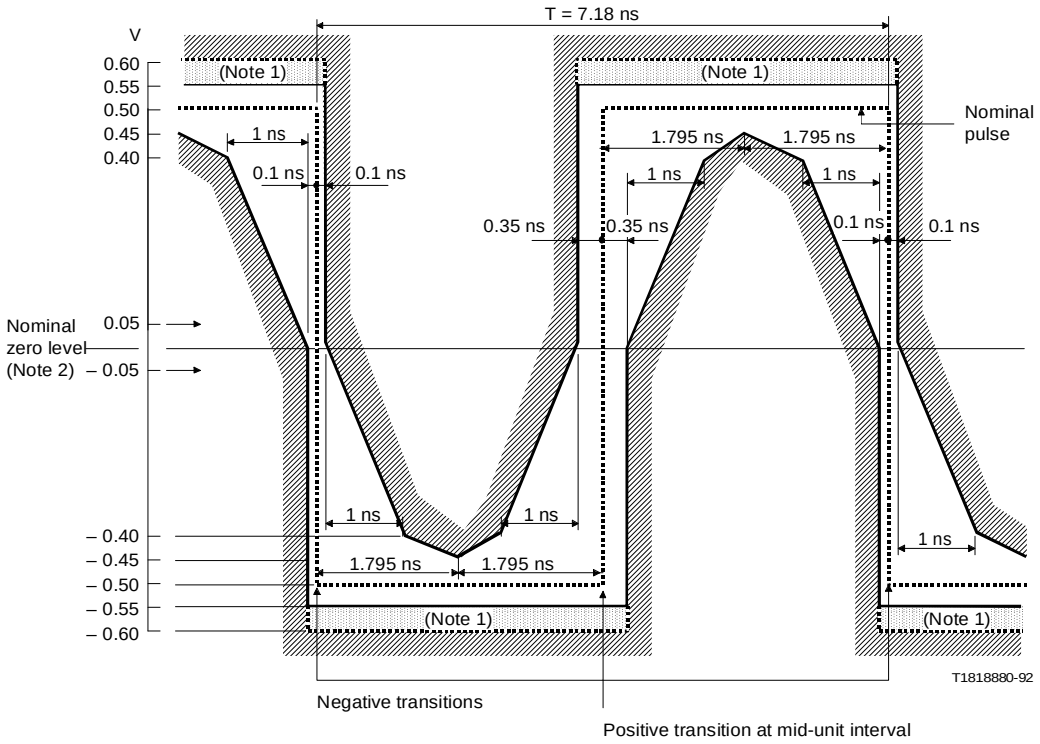
The attenuation of the coaxial pair should be assumed to follow an approximate $\sqrt{f}$ law and to have a maximum insertion loss of 12 dB at a frequency of 70 MHz.

For the jitter to be tolerated at the input port refer to § 3 of Recommendation G.823.

The return loss characteristics should be the same as that specified for the output port.

9.4 *Earthing of outer conductor or screen*

The outer conductor of the coaxial pair shall be connected to the earth at the output port, and provision shall be made for connecting this conductor to earth, if required, at the input port.



Note 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

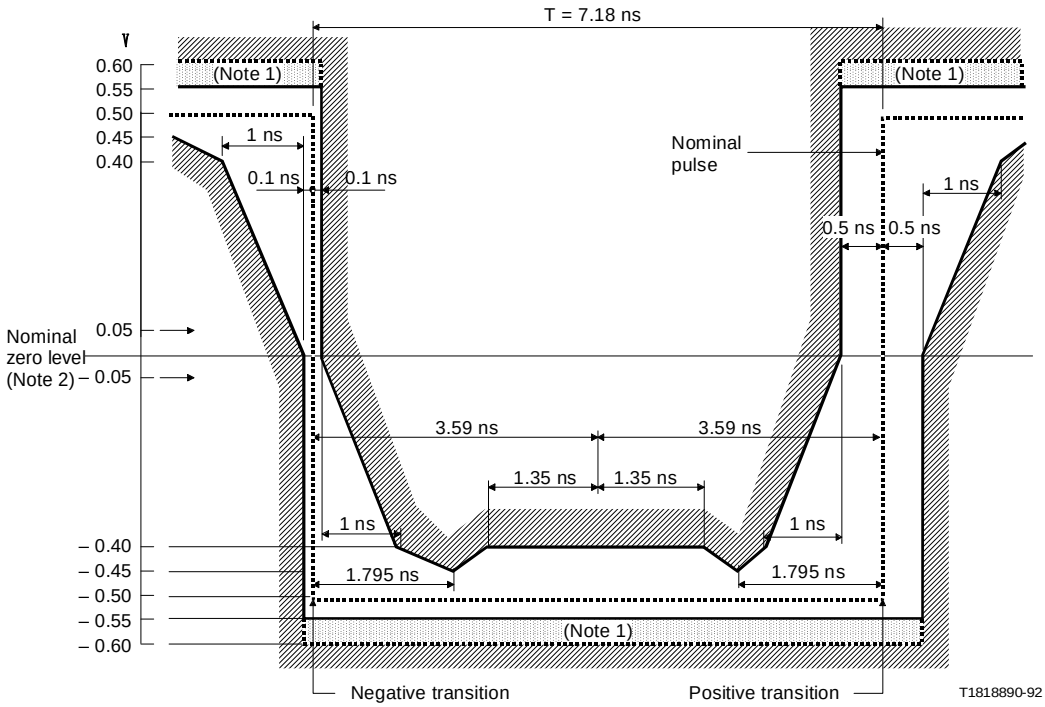
Note 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 μF, to the input of the oscilloscope used for measurements.
The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ± 0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ± 0.05 V of the nominal zero level of the masks.

Note 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.
The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.
When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].
These techniques require further study.

Note 4 – For the purpose of these masks, the rise time and decay time should be measured between – 0.4 V and 0.4 V, and should not exceed 2 ns.

FIGURE 19/G.703

Mask of a pulse corresponding to a binary 0



Note 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

Note 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 μF, to the input of the oscilloscope used for measurements.
The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ± 0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ± 0.05 V of the nominal zero level of the masks.

Note 3 – Each pulse in a coded sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.
The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.
When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].
These techniques require further study.

Note 4 – For the purpose of these masks, the rise time and decay time should be measured between – 0.4 V and 0.4 V, and should not exceed 2 ns.

Note 5 – The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions are ± 0.1 ns and ± 0.5 ns respectively.

FIGURE 20/G.703
Mask of a pulse corresponding to a binary 1

10 2048 kHz synchronization interface

10.1 *General*

The use of this interface is recommended for all applications where it is required to synchronize a digital equipment by an external 2048 kHz synchronization signal.

Overvoltage protection requirement: see Annex B.

10.2 *Specifications at the output port*

See Table 10/G.703.

TABLE 10/G.703

Frequency	2048 kHz ± 50 ppm	
Pulse shape	The signal must conform with the mask (Figure 21/G.703) The value V corresponds to the maximum peak value The value V_1 corresponds to the minimum peak value	
Type of pair	Coaxial pair (see Note in § 10.3)	Symmetrical pair (see Note in § 10.3)
Test load impedance	75 ohms resistive	120 ohms resistive
Maximum peak voltage (V_{op})	1.5	1.9
Minimum peak voltage (V_{op})	0.75	1.0
Maximum jitter at an output port	0.05 IU peak-to-peak, measured within the frequency range f_1 = 20 Hz to f_4 = 100 kHz (Note)	

Note – This value is valid for network timing distribution equipments. Other values may be specified for timing output ports of digital links carrying the network timing.

10.3 *Specifications at the input ports*

The signal presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pair.

The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 2048 kHz should be in the range 0 to 6 dB (minimum value). This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

The input port shall be able to tolerate a digital signal with these electrical characteristics but modulated by jitter. The jitter values are under study.

The return loss at 2048 kHz should be ≥ 15 dB.

Note – The outer conductor of the coaxial pair or the screen of the symmetrical pair shall be connected to earth at the output port, and provision shall be made for connecting the outer conductor of the coaxial pair or the screen of the symmetrical pair to earth if required, at the input port.

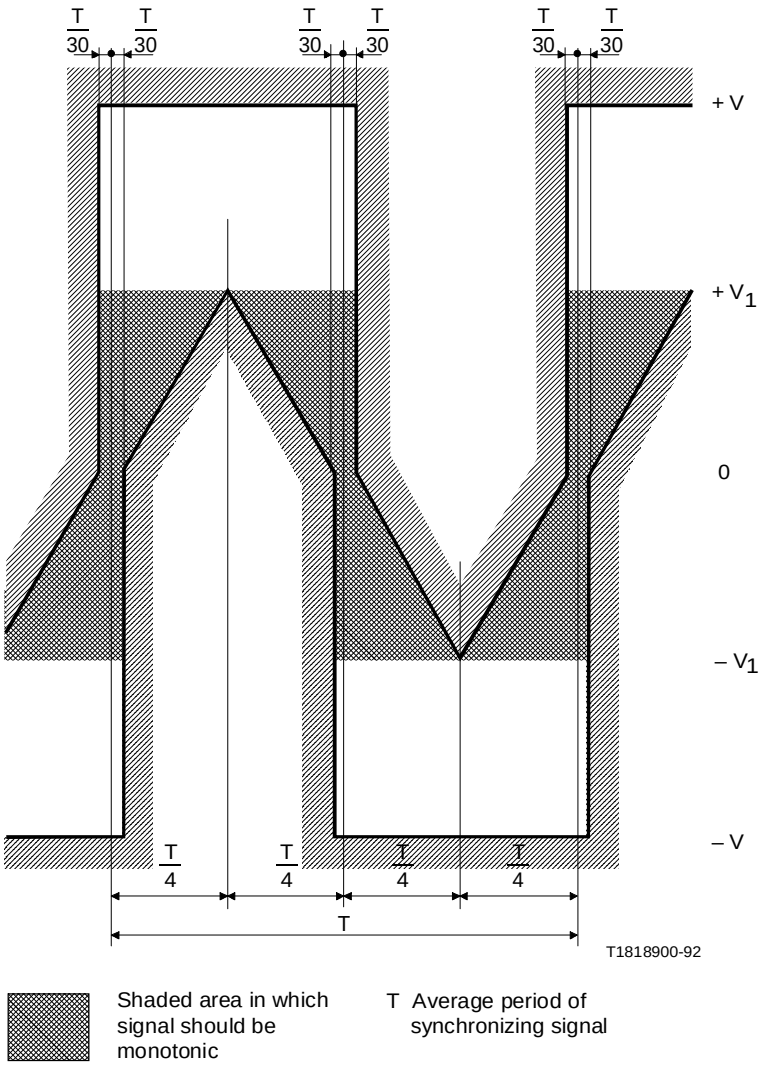


FIGURE 21/G.703

Wave shape at an output port

11 Interface at 97 728 kbit/s

11.1 Interconnection of 97 728 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

11.2 The signal shall have a bit rate of 97 728 kbit/s ± 10 ppm.

11.3 One coaxial pair shall be used for each direction of transmission.

11.4 The test load impedance shall be 75 ohms ± 5% resistive.

11.5 A scrambled AMI code[1)] shall be used.

---

1) An AMI code is scrambled by a five-stage reset-type scrambler with the primitive polynominal of $x^5 + x^3 + 1$.

11.6 The shape for the 97 728 kbit/s output port shall fall within the mask in Figure 22/G.703. The shape at the point where the signal arrives at the distribution frame will be modified by the characteristics of the interconnecting cable.

11.7 The connectors and cable pairs in the distribution frame shall be 75 ohms ± 5%.

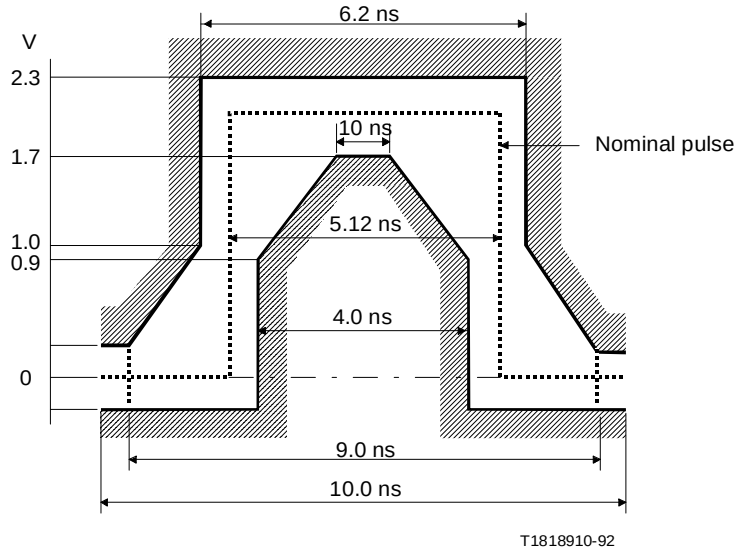


FIGURE 22/G.703

Pulse mask at the 97 728 kbit/s output port

12 Interface at 155 520 kbit/s

12.1 *General characteristics*

Bit rate: 155 520 kbit/s

Bit rate tolerance: ± 20 ppm

Code: Coded mark inversion (CMI)

Overvoltage protection requirement: See Annex B.

CMI is a two level non-return-to-zero code in which binary 0 is coded such that both amplitude levels, A_1, and A_2, are attained consecutively, each for half a unit time interval (T/2).

Binary 1 is coded by either of the amplitude levels A_1 or A_2, for one full unit time interval (T), in such a way that the level alternates for successive binary 1s.

An example is given in Figure 23/G.703.

Note 1 – For binary 0, there is always a positive transition at the midpoint of the binary unit time interval.

Note 2 – For binary 1:

a) there is a positive transition at the start of the binary unit time interval if in the preceding time interval the level was A_1;

b) there is a negative transition at the start of the binary unit time interval if the last binary 1 was encoded by level A_2.

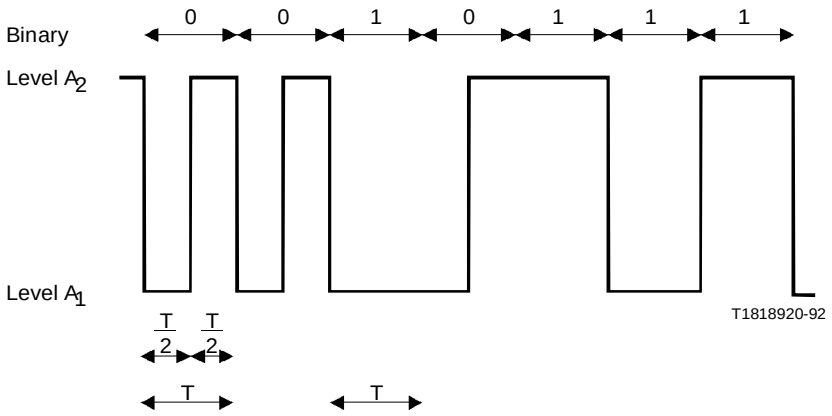


FIGURE 23/G.703

Example of CMI coded binary signal

12.2 *Specifications at the output ports*

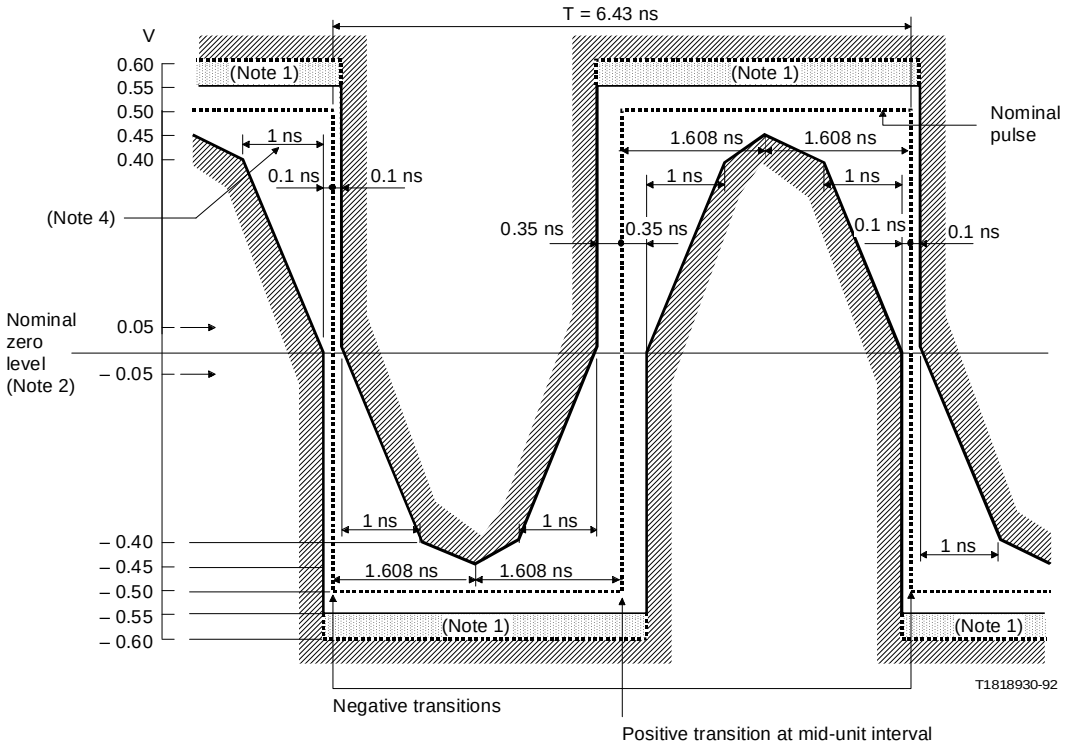
The specifications at the output ports are given in Table 11/G.703 and Figures 24/G.702 and 25/G.702.

Note – A method based on the measurement of the levels of the fundamental frequency component, the second (and possibly the third) harmonic of a signal corresponding to the binary all 0s and binary all 1s, is considered to be a perfectly adequate method of checking that the requirements of Table 11/G.703 have been met. The relevant values of the harmonic components are under study.

TABLE 11/G.703

Specifications at the output ports

Pulse shape	Nominally rectangular and conforming to the masks shown in Figures 24/G.703 and 25/G.703
Pair(s) in each direction	One coaxial pair
Test load impedance	75 ohms resistive
Peak-to-peak voltage	1 ± 0.1 volt
Rise time between 10% and 90% amplitudes of the measured steady state amplitude	≤ 2 ns
Transition timing tolerance referred to the mean value of the 50% amplitude points of negative transitions	Negative transitions: ± 0.1 ns Positive transitions at unit interval boundaries: ± 0.5 ns Positive transitions at mid-unit intervals: ± 0.35 ns
Return loss	≥ 15 dB over frequency range 8 MHz to 240 MHz
Maximum peak-to-peak jitter at an output port	Under study



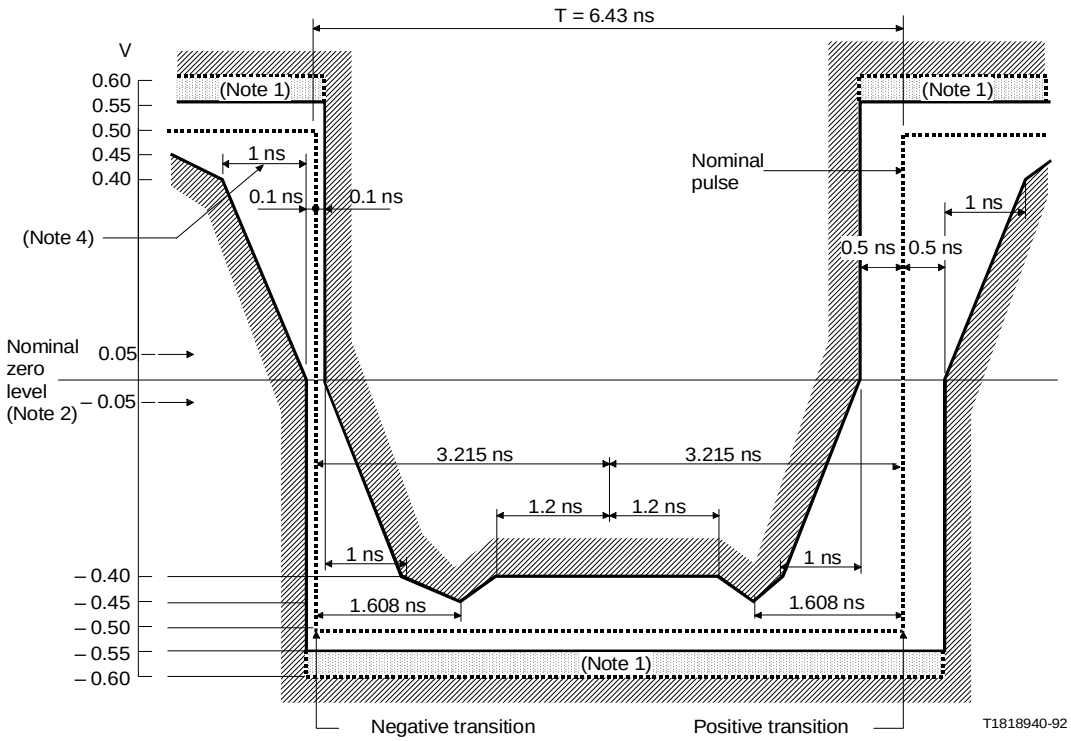
Note 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

Note 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 μF, to the input of the oscilloscope used for measurements.
The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ± 0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ± 0.05 V of the nominal zero level of the masks.

Note 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.
The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.
When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].
These techniques require further study.

Note 4 – For the purpose of these masks, the rise time and decay time should be measured between – 0.4 V and 0.4 V, and should not exceed 2 ns.

FIGURE 24/G.703
Mask of a pulse corresponding to a binary 0
(Note 3)



Note 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

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The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ± 0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ± 0.05 V of the nominal zero level of the masks.

Note 3 – Each pulse in a coded sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.
The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.
When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].
These techniques require further study.

Note 4 – For the purpose of these masks, the rise time and decay time should be measured between – 0.4 V and 0.4 V, and should not exceed 2 ns.

Note 5 – The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions are ± 0.1 ns and ± 0.5 ns respectively.

FIGURE 25/G.703
Mask of a pulse corresponding to a binary 1
(Notes 3 and 5)

12.3 *Specifications at the input ports*

The digital signal presented at the input port should conform to Table 11/G.703 and Figures 24/G.703 and 25/G.703 modified by the characteristics of the interconnecting coaxial pair.

The attenuation of the coaxial pair should be assumed to follow an approximate $\sqrt{f}$ law and to have a maximum insertion loss of 12.7 dB at a frequency of 78 MHz.

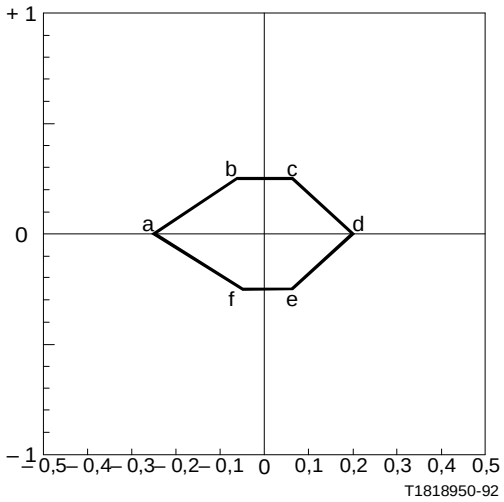
Jitter to be tolerated at the input port is under study.

The return loss characteristics should be the same as that specified for the output port.

12.4 *Specifications at the cross-connect points*

– *Signal power level:* A wideband power measurement using a power level sensor with a working frequency range of at least 300 MHz shall be between –2.5 and +4.3 dBm. There shall be no d.c. power transmitted across the interface.

– *Eye diagram:* An eye diagram mask based on the maximum and minimum power levels given above is shown in Figure 26/G.703 where the voltage amplitude has been normalized to one, and the time scale is specified in terms of the pulse repetition period T. The corner points of the eye diagram are shown in Figure 26/G.703.



Point	Time	Amplitude
a	–0.25 T/2	0.00
b	–0.05 T/2	0.25
c	–0.05 T/2	0.25
d	–0.20 T/2	0.00
e	–0.05 T/2	–0.25
f	–0.05 T/2	–0.25

FIGURE 26/G.703

STM-1 interface eye diagram

– *Termination:* One coaxial cable shall be used for each direction of transmission.

– *Impedance:* A resistive test load of 75 ohms ± 5% shall be used at the interface for the evaluation of the eye diagram and the electrical parameters of the signal.

12.5 *Earthing of outer conductor or screen*

The outer conductor of the coaxial pair shall be connected to the Earth at the output port, and provision shall be made for connecting this conductor to Earth, if required, at the input port.

ANNEX A

(to Recommendation G.703)

Definition of codes

This annex defines the modified alternate mark inversion codes (see Recommendation G.701, item 9005) whose use is specified in this Recommendation.

In these codes, binary 1 bits are generally represented by alternate positive and negative pulses, and binary 0 bits by spaces. Exceptions, as specified for the individual codes, are made when strings of successive 0 bits occur in the binary signal.

In the definitions below, B represents an inserted pulse conforming to the AMI rule (Recommen-dation G.701, item 9004), and V represents an AMI violation (Recommendation G.701, item 9007).

The encoding of binary signals in accordance with the rules given in this annex includes frame alignment bits, etc.

A.1 *Definition of B3ZS (also designated HDB2) and HDB3*

Each block of 3 (or 4) successive zeros is replaced by 00V (or 000V respectively) or B0V (B00V). The choice of 00V (000V) or B0V (B00V) is made so that the number of B pulses between consecutive V pulses is odd. In other words, successive V pulses are of alternate polarity so that no d.c. component is introduced.

Note – The abbreviations stand for the following:

HDB2 (HDB3) high density bipolar of order 2 (3)

B3ZS bipolar with three-zero substitution.

A.2 *Definition of B6ZS and B8ZS*

Each block of 6 (or 8) successive zeros is replaced by 0VB0VB (or 000VB0VB respectively).

ANNEX B

(to Recommendation G.703)

Specification of the overvoltage protection requirement

The input and output ports should withstand without damage the following tests:

– 10 standard lightning impulses (1.2/50 μs) with a maximum amplitude of U (5 negative and 5 positive impulses). For the definition of this impulse see [1].

– at the interface for coaxial pairs:
  i) differential mode: with a pulse generator of Figure B-1/G.703, the value of U is under study;
  ii) common mode – under study;
– at the interface for symmetrical pairs:
  i) differential mode: with a pulse generator of Figure B-1/G.703, the value of U is under study (a value of 20 V has been mentioned);
  ii) common mode: with a pulse generator of Figure B-2/G.703, U = 100 V_{dc}.

Possible pulse generators are described in Figures B-1/G.703 and B-2/G.703.

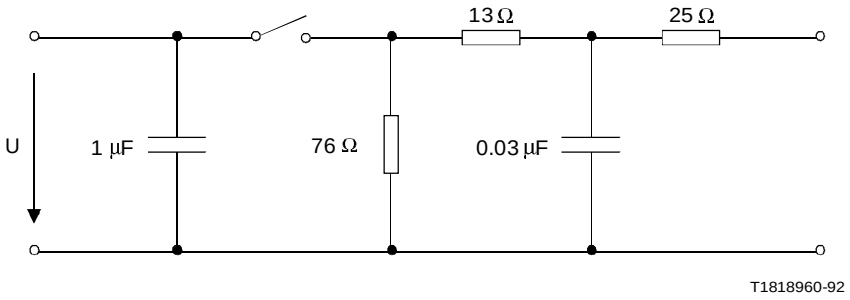


FIGURE B-1/G.703
Pulse generator 1.2/50 ms for differential mode voltages

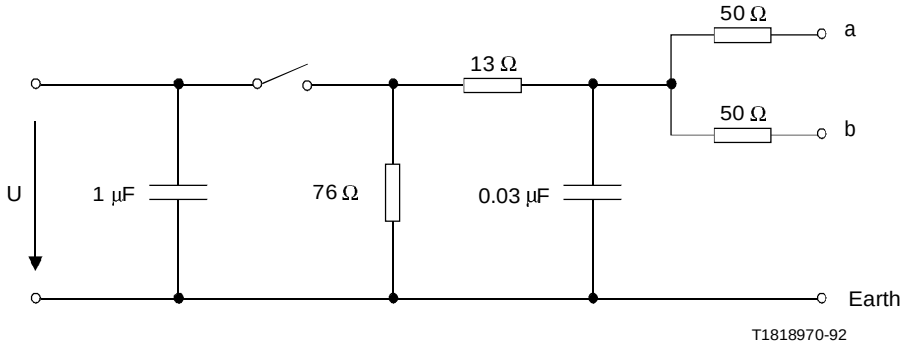


FIGURE B-2/G.703

Pulse generator 1.2/50 ms for common mode voltages at symmetrical interfaces

References

[1] IEC publication No. 60-2 *High-voltage test techniques, Part 2: Test procedures*, Geneva, 1973.

ANNEX C

(to Recommendation G.703)

Alphabetical list of abbreviations used in this Recommendation

AIS	Alarm indication of signal
B3ZS	Bipolar with three-zero substitution
CMI	Coded mark inversion
HDB2	High density bipolar of order 2 code
HDB3	High density bipolar of order 3 code